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produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.

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Important Information. Xilinx introduces the first release of the Vitis™ Unified Software Platform in 2019.2. Unification of Xilinx SDK, SDSoC™ and SDAccel™ Development Environment into an all-in-one software platform for embedded software and application acceleration development

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